In The Claims

1-5 (Cancelled)

6. (Previously Presented) A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

a first plurality of vias, each having a top end and a bottom end;

a second plurality of vias, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping;

a first routing level at a first height, said first level connected to the first plurality of vias at the bottom end of each first via; and

a second routing level at a second height, said second level connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height,

wherein both routing levels are formed above a substrate,

wherein the first and second vias are evenly spaced and have a common first pitch,

and further comprising a third routing level, the third routing level above the first and second vias connected at the top end of each first and second via,

vertically opposite the first and second routing levels,

wherein the third routing level comprises memory lines in a memory array, and wherein the first plurality of vias are not connected to any routing level above the first routing level and below the third routing level, and wherein the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level.

7. (Original) The structure of claim 6 wherein memory cells accessed by the memory lines are charge storage memory cells.

8. (Original) The structure of claim 7 wherein the memory cells are SONOS devices.

9. (Original) The structure of claim 7 wherein the memory cells are floating gate devices.

10. (Original) The structure of claim 7 wherein the memory cells are arranged in a NAND string.

11. (Original) The structure of claim 6 wherein memory cells accessed by the memory lines are passive element memory cells.

12. (Original) The structure of claim 11 wherein at least one passive element memory cell comprises an antifuse.

13. (Original) The structure of claim 11 wherein at least one passive element memory cell comprises a fuse.

14. (Original) The structure of claim 6 wherein the memory array is a monolithic three dimensional memory array.

15. (Previously Presented) The structure of claim 6 wherein the memory lines have a fourth pitch smaller than the first pitch.

16-26 (Cancelled)

27. (Original) The structure of claim 6 wherein the array is a monolithic three dimensional memory array comprising at least first and second memory levels, the second memory level formed vertically above the first memory level.

28-32 (Cancelled)

33. (Previously Presented) A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

a first plurality of vias, each having a top end and a bottom end;

a second plurality of vias, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping;

a first routing level at a first height, said first level connected to the first plurality of vias at the bottom end of each first via;

a second routing level at a second height, said second level connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height; and

a third routing level at a third height, the third level connected to the first plurality of vias and to the second plurality of vias at the top end of each first and second via, wherein all three routing levels are formed above a substrate,

wherein the first and second vias are evenly spaced and have a first pitch, wherein the third routing level comprises memory lines in a memory array, and

wherein the first plurality of vias are not connected to any routing level above the first routing level and below the third routing level, and wherein the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level.

34. (Original) The structure of claim 33 wherein the first routing level has a second pitch, the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

35. (Original) The structure of claim 34 wherein memory cells accessed by the memory lines are charge storage memory cells.

36. (Original) The structure of claim 35 wherein the memory cells are SONOS devices.

37. (Original) The structure of claim 35 wherein the memory cells are floating gate devices.

38. (Original) The structure of claim 35 wherein the memory cells are arranged in a NAND string.

39. (Original) The structure of claim 34 wherein memory cells accessed by the memory lines are passive element memory cells.

40. (Original) The structure of claim 39 wherein at least one passive element memory cell comprises an antifuse.

41. (Original) The structure of claim 39 wherein at least one passive element memory cell comprises a fuse.

42. (Original) The structure of claim 33 wherein the memory array is a monolithic three dimensional memory array.

43. (Original) The structure of claim 33 wherein the memory lines have a fourth pitch smaller than the first pitch.

44-54 (Cancelled)

55. (Previously Presented) A structure for providing multilevel electrical connectivity within a memory array, the structure comprising:

a first plurality of vias, each having a top end and a bottom end;

a second plurality of vias, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping;

a first routing level at a first height, said first level connected to the first plurality of vias at the top end or the bottom end of each first via;

a second routing level at a second height, said second level connected to the second plurality of vias at the top end or bottom end of each second via, wherein the first height is different from the second height; and

a third routing level at a third height, the third level connected to the first plurality of vias and to the second plurality of vias at the top end or the bottom end of each first or second via, vertically opposite the first or second routing level, where all three routing levels are formed above a substrate,

wherein the first and second vias are evenly spaced and have a first pitch, wherein the array is a monolithic three dimensional memory array comprising at least first and second memory levels, the second memory level formed vertically above the first memory level, and

wherein the first plurality of vias are not connected to any routing level vertically between the first routing level and the third routing level, and wherein the second plurality of vias are not connected to any routing level vertically between the second routing level and the third routing level.

56-58 (Cancelled)

59. (Previously Presented) A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

a first plurality of vias, each having a top end and a bottom end;

a second plurality of vias, each having a top end and a bottom end;

a first routing level at a first height, said first level connected to the first plurality of vias at the bottom end of each first via;

a second routing level at a second height, said second level connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height; and

a third routing level at a third height, the third level connected to the first plurality of vias and to the second plurality of vias at the top end of each first and second via, wherein all three routing levels are formed above a substrate,

wherein the first and second vias are evenly spaced and have a first pitch, wherein the third routing level comprises memory lines in a memory array, and

wherein the first plurality of vias are not connected to any routing level above the first routing level and below the third routing level, and wherein the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level.

60. (Original) The structure of claim 59 wherein the first routing level has a second pitch, the second routing level has a third pitch, the first pitch smaller than the second pitch and the third pitch.

61. (Original) The structure of claim 60 wherein memory cells accessed by the memory lines are charge storage memory cells.

62. (Original) The structure of claim 61 wherein the memory cells are SONOS devices.

63. (Original) The structure of claim 61 wherein the memory cells are floating gate devices.

64. (Original) The structure of claim 61 wherein the memory cells are arranged in a NAND string.

65. (Original) The structure of claim 60 wherein memory cells accessed by the memory lines are passive element memory cells.

66. (Original) The structure of claim 65 wherein at least one passive element memory cell comprises an antifuse.

67. (Original) The structure of claim 65 wherein at least one passive element memory cell comprises a fuse.

68. (Original) The structure of claim 59 wherein the memory array is a monolithic three dimensional memory array.

69. (Original) The structure of claim 59 wherein the memory lines have a fourth pitch smaller than the first pitch.

70-72 (Cancelled)

73. (Previously Presented) A structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising:

a first plurality of vias, each having a top end and a bottom end;

a second plurality of vias, each having a top end and a bottom end;

a first routing level at a first height, said first level connected to the first plurality of vias at the top or bottom end of each first via;

a second routing level at a second height, said second level connected to the second plurality of vias at the top or bottom end of each second via, wherein the first height is different from the second height; and

a third routing level at a third height, the third level connected to the first plurality of vias and to the second plurality of vias at the top or bottom end of each first and second via, vertically opposite the first or second routing level, wherein all three routing levels are formed above a substrate, wherein the first and second vias are evenly spaced and have a first pitch,

wherein the integrated circuit comprises a memory array,

wherein the memory array is monolithic three dimensional memory array comprising at least first and second memory levels, the second memory level formed vertically above the first memory level, and

wherein the first plurality of vias are not connected to any routing level vertically between the first routing level and the third routing level, and wherein the second plurality of vias are not connected to any routing level vertically between the second routing level and the third routing level.

74-82 (Cancelled)

83. (Previously Presented) A method for forming a via and routing structure for electrically connecting a multilevel array in an integrated circuit, the method comprising:

forming a first routing level;

forming a second routing level above the first routing level;

forming a first plurality of vias connected at bottom ends to the first routing level;

forming a second plurality of vias connected at bottom ends to the second routing level, wherein the first and second pluralities of vias are vertically overlapping,

wherein the multilevel array comprises a row of vias having a first pitch, the row of vias comprising the first plurality of vias and the second plurality of vias,

vias of the first and second pluralities interspersed,

further comprising forming a third routing level above the first and second routing levels, wherein

said third routing level connects to top ends of the first plurality of vias or

said third routing level connects to top ends of the second plurality of vias,

wherein the third routing level comprises memory lines in a memory array, and wherein the first plurality of vias are not connected to any routing level above the first routing level and below the third routing level, and where the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level.

84. (Original) The method of claim 83 wherein the first routing level has a second pitch larger than the first pitch.

85. (Original) The method of claim 84 wherein the memory lines have a third pitch smaller than the first pitch.

86. (Original) The method of claim 83 wherein memory cells accessed by the memory lines are charge storage memory cells.

87. (Original) The method of claim 86 wherein the memory cells are SONOS devices.

88. (Original) The method of claim 86 wherein the memory cells are floating gate devices.

89. (Original) The method of claim 86 wherein the memory cells are arranged in a NAND string.

90. (Original) The method of claim 83 wherein the memory array is a monolithic three dimensional memory array.

91. (Original) The method of claim 83 wherein memory cells accessed by the memory lines are passive element memory cells.

92. (Original) The method of claim 91 wherein at least one passive element memory cell comprises an antifuse.

93. (Original) The method of claim 91 wherein at least one passive element memory cell comprises a fuse.

94 (Cancelled)